REMARKS

The applicants have studied the Office Action dated October 27, 2003. It is submitted that the application is in condition for allowance. Claims 1, 11, 12, 14, 20 and 29 have been amended and claims 7, 16, 25 and 30 have been canceled without prejudice or disclaimer. Reconsideration and allowance of all of the claims in view of the following remarks are respectfully requested.

Claims 1-2, 4-5, 7-22 and 25-29 were rejected under 35 U.S.C. 102(b) as being anticipated by Tolson et al. (GB 2,343,572).

Claims 3 and 23 were rejected under 35 U.S.C. 103(a) as being unpatentable over Tolson in view of Andersen et al. (US 5,442,663). These rejections are respectfully traversed.

The amended claim 1 recites "an adder circuit to receive the combined signal and the filtered signal to thereby remove the jammer signal therefrom, wherein the adder circuit comprises a positive and negative input, the combined signal being coupled to the positive input and the filtered signal being coupled to the negative input." Other independent claims recite a similar language. The Tolson and Andersen references do not disclose an adder circuit having a combined signal (jammer + desired) coupled to its positive input and the filtered jammer signal coupled to its negative input, as recited in the claims.

In the Tolson reference, the adder 5 only has positive inputs and does not have a negative input coupled to a filted jammer signal. In the Tolson reference, unwanted signals from filters 10 and 11 are phase shifted by the phase shifter 13 by 180 degrees so that the unwanted signals outputted by the phase shifter 13 have a complete anti-phase to the unwanted signals outputted by the mixer 3. As a result, the unwanted signals from the phase shifter 13 cancels the unwanted signals from the mixer 3 when they are added together by the adder 5 since the unwanted signals from the phase shifter 13 have an opposite phase to the unwanted signals from the mixer 3. Therefore, the adder 5 does not have a negative input that is coupled to a filtered jammer signal. The adder 5 only has positive inputs since the unwanted signals from the phase shifter 13 are already phase shifted before being inputted into the adder 5.

Thus, the Tolson reference does not disclose an adder circuit having a combined signal (jammer + desired) coupled to its positive input and the filtered jammer signal coupled to its negative input, as recited in the claims.

The Andersen reference does not address the deficiencies of the Tolson reference.

Therefore, it is respectfully submitted that the rejection of the claims under 35 U.S.C. §102 and 103 should be withdrawn.

The Examiner stated that claim 30 would be allowable if it was re-written in an independent form. The limitations of claim 30 have been incorporated into claim 29. Thus, claim 29 is now allowable.

The applicants thank the Examiner for allowing claims 31-34.

In view of the foregoing, it is respectfully submitted that the application and all of the claims are in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If there are any fees due in connection with the filing of this response, please charge such fees to our Deposit Account No. 17-0026. If a fee is required for an extension of time under 37 C.F.R. 1.136 not accounted for, such an extension is requested and the fee should also be charged to our Deposit Account. A duplicate copy of this page is enclosed.

Respectfully submitted,

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